ABSTRACT OF THE DISCLOSURE

An Extending circuit for memory comprises: an output data effective signal generator 2 for, when a status signal STNF from a next-stage FIFO circuit represents a data writable state, asserting a write enable signal NWEO from the next-stage FIFO circuit, and enabling data to be written into the next-stage FIFO circuit; and an internal FIFO write enable generator 3 for receiving a status signal STNF from the next-stage FIFO circuit, when the next-stage FIFO circuit is in a data unwritable state, asserting an internal FIFO write enable signal S3, and enabling data to be written into the internal FIFO circuit 1.